

Electronics System Integration Technology Conferences ESTC 2010 in Berlin

Advance Program

September 13–16, 2010, Berlin Maritim Pro Arte





Welcome to ESTC 2010!

Organized by IEEE-CPMT since 2006, the Electronics System Integration Technology Conferences ESTC conference series has become the premier venue for academics and industry to present and discuss the latest developments in assembly and interconnection technology and new applications. Just like its highly successful predecessor events in Dresden (2006) and Greenwich (2008) ESTC 2010 will again feature a powerful technical program, with 160 oral and 90 poster presentations in five parallel sessions. I would like to extend a big thank you to all who submitted a paper or poster for helping to ensure that the conference will be a great success.

ESTC always hosts cutting-edge workshops on select topics in microelectronic packaging. For more information on this year's tutorials as well as a special full-day website please refer to our website at www.estc-2010.de. There you will also find updated information about the program, the social events and the technical tours.

Apart from the opportunity to participate in what we believe will be some truly inspiring research presentations, on a personal level we also hope ESTC 2010 will be a chance for us to meet new cooperation partners and reconnect with trusted colleagues. So please, join us for a perfect late summer conference at ESTC in Berlin and bring your ideas, comments and suggestions – anything at all that you feel will help us provide a better service to you.

We look forward to seeing you in September!

Rolf Aschenbrenner
General Conference Chair

Klaus-Dieter Lang
Executive Chair

The organizers are delighted to welcome four distinguished colleagues from industry and science as keynote speakers at the ESTC 2010 Conference. Eric Saugier (ST Microelectronics, Singapore), Eduardo Fernández (University Miguel Hernandez, Spain), Reinhard Ploss (Infineon AG, Germany) and Kiyoshi Arita (Panasonic, Japan) will showcase their latest research results and discuss the importance of packaging trends and system integration in their companies. Together, their presentations will provide an exciting overview of electronic system integration today and afford a glimpse of where research and industry is heading.



KEYNOTE: Packaging Trends in Mobile Electronics – Towards Wafer Level Packaging

Eric Saugier

STMicroelectronics, Corporate Packaging & Automation

Eric Saugier is managing the BGA advanced packaging at STMicroelectronics. He graduated with a Master Degree in Mechanical Engineering from the French National Institute of Applied Sciences (INSA). After working for Tyco Electronics on connector R&D, he joined ST in 2002 where he initially managed the camera module packaging development. Since 2008 he is in charge of the BGA advanced packaging in the central packaging development group of ST.



KEYNOTE: Micro-technologies for New Neural Interfaces: Current Status and Future Prospects

Eduardo Fernandez

Bioengineering Institute and CIBER-BBN, University Miguel Hernandez, Spain

Eduardo Fernandez is Professor of Cellular Biology and Chairman of the Department of Histology and Anatomy in the University Miguel Hernández (Spain), Director of the Neuroengineering and Neuroprosthesis Unit and also serves as Co-Director of the Bioengineering Institute. He received a M.D. degree from the University of Alicante (1986) and a Ph.D. in Neuroscience with honors in 1990. He has been visiting professor at the University of Utah (USA), University of Oldenburg (Germany), Beth Israel Medical Deaconess Center (USA) and University of Vienna (Austria).



KEYNOTE: Growing Importance of System Integration

Dr. Reinhard Ploss

Member of the Management Board Infineon Technologies AG

Reinhard Ploss joined Siemens/Infineon in 1986 as a process engineer for ion implantation in wafer manufacture at Munich. He worked in various positions at Infineon since then and in 2000 became head of the Automotive & Industrial Business Group, which then encompassed power semiconductors, electric drives, automotive applications and the Microcontroller Business Unit. In 2005 Reinhard Ploss assumed responsibility for manufacture, development and operational management in the Automotive, Industrial and Multimarket Business Group. In June 2007, Dr. Reinhard Ploss became a member of the management board and is now responsible for Operations comprising central manufacturing Frontend and Backend, Test, Quality Management as well as Logistics.



KEYNOTE: Latest Panasonic Packaging Technology and Solutions

Kiyoshi Arita

Panasonic Factory Solutions

Kiyoshi Arita, received his Doctor's degree from Kyushu Institute of Technology in 1998 and MBA's degree from Kyushu University in 2008. He majored in plasma processes for semiconductor manufacturing and bonding processes for packaging. He developed a wire bonder, copper wire bonder, stud bump bonder, inner lead bonder, plasma cleaner, plasma stress relief system and plasma dicer since he joined Panasonic Factory Solutions. His recent experience as general manager includes development of a dry etcher for high power LED elements.

		Hall B	Hall C	Salon 2	Salon 3	Salon 4
Monday, Sept. 13, 2010	09.00 – 06.00 pm	Workshop @ Fraunhofer IZM				
	12.30 – 01.30 pm	Lunch				
	01.30 – 05.00 pm	Tutorial 4 [Fraunhofer IZM]		Tutorial 1	Tutorial 3	
	04.00 – 06.00 pm	Chinese Session				
Tuesday, Sept. 14, 2010	08.30 – 09.30 am	Check-in				
	09.30 – 10.00 am	Opening				
	10.00 – 12.00 pm	Keynotes a 40 min.				
	12.00 – 01.20 pm	Exhibition Opening + Lunch				
	01.20 – 03.00 pm	MS-1	AP-1	AR-1	ED-1	AM-1
	03.00 – 04.00 pm	Coffee break & Poster Session 1 [Hall A]				
	04.00 – 05.40 pm	MS-2	AP-2	AR-2	ED-2	AM-2
	06.00 – 07.30 pm	Reception in the ESTC Exhibition Area - Berliner Abend [Hall 2]				
	07.30 – 09.00 pm	Panel Discussion				
Wednesday, Sept. 15, 2010	08.30 – 10.10 am	MS-3	MP-1	AR-3	NM-1	AM-3
	10.10 – 11.00 am	Coffee break & Poster Session 2 [Hall A]				
	11.00 – 12.40 pm	MS-4	MP-2	ET-1	NM-2	AM-4
	12.40 – 02.00 pm	Lunch Buffet @ Exhibition [Hall 2]				
	02.00 – 03.40 pm **	MS-5	MP-3	ET-2	NM-3	AM-5
	03.40 – 04.30 pm	Coffee break & Poster Session 3 [Hall A]				
	04.30 – 06.10 pm	MS-6	AP-3	AR-4	NM-4	AM-6
	07.00 – 09.00 pm	Gala Dinner @ Meilenwerk				
Thursday, Sept. 16, 2010	08.30 – 10.10 am	NM-5	AP-4	AR-5	OE-1	PE-1
	10.10 – 11.00 am	Coffee break & Poster Session 4 [Hall A]				
	11.00 – 12.40 pm	NM-6	AP-5	AR-6	OE-2	PE-2
	12.40 – 01.40 pm	Lunch Buffet @ Exhibition				
	01.40 – 02.20 pm	Keynote				
	02.20 – 02.50 pm	Paper Award				
	02.50 – 03.20 pm	Closing				
	03.20 – 09.00 pm	iNemi Wokshop				
Friday, Sept. 17, 2010	09.00 – 12.30 am	Technical Tour ESTC meets IZM				
	08.30 – 03.30 pm	iNEMI Workshop				

** Wednesday, Sept 15, 2010, 02.00–3.40 pm: **IMAPS Europe's Global Business Council // Salon 6**

Program Highlights from ESTC 2010

Monday, September 13, 2010

09.00 am

Full-Day Workshop on 3D Wafer Level Packaging

M. Jürgen Wolf of Fraunhofer IZM and Ehrenfried Zschech of Fraunhofer IZFP-D have organized a high-level one-day-workshop on 3D wafer level packaging, bringing together experts on 3D WLP from all over the world. The focus of the workshop will be on 3D roadmapping, 3D technology aspects and 3D interconnect process control and quality engineering.

1.30 pm

Half-Day Tutorials

ESTC always hosts cutting-edge workshops on select topics in microelectronic packaging. This year's half-day workshops are on 1st and 2nd level packaging testing, system integration reliability, and harsh environment packaging using polymers. These events can be booked separately. Check our website for more information.

- **Tutorial: Testing for 1st and 2nd Level Electronics Packaging**
Instructor: Klaus-Jürgen Wolter, TU Dresden
- **Tutorial: Reliability for System Integration**
Instructor: Bernhard Wunderle, Fraunhofer IZM, Berlin, TU Chemnitz
- **Tutorial: Harsh Environment Packaging Using Polymers**
Instructor: Karl-Friedrich Becker, Fraunhofer IZM, Berlin

4.00 pm

Chinese Session

Prof. Keyun Bi is organizing a special "Chinese Session" on the afternoon of September 13. Join us to learn more about China's contribution to developments and applications in packaging technologies.

Chair: Prof. Keyun Bi

President of EMPT-CIE, Packaging Branch of CSIA

Title: The Development of IC Packaging Industry of China

Speakers:

Dr. Hao Tang

Director of Technology, Nantong Fujitsu Microelectronics Co., Ltd

Title: Advanced Semiconductor Packaging Solutions from QFN to 3D, WLP and more

Wade Lam

Chairman of Grand Tech Group Ltd

Title: Grand Tech Group, Your Automation Solution And Innovation Partner

Dr. Weiping Li

Corporate VP, New Technologies and US & Europe Markets, Jiangsu Changjian Electronics Technology Co., Ltd (JCET)

Title: MIS Package – The New Generation Packaging Technology for High-Performance Applications

Prof. Zhiyue Wang

Deputy Director General of the 45th Research Institute of Chinese Electronic Technology Group Company (CETC)

Title: The Status Quo and Developing Trend of Chinese Packaging Equipment Industry for IC

Dr. Wenhui Zhu

CTO of Tian Shui Hua Tian Technology Co., Ltd

Title: Development of LGA-SiP and Leadframe Based Advance Packaging

Tuesday, September 14, 2010
09.30 am – 03.00 pm

- 09:30 am** **Opening: Introduction and Welcome to the third Electronics System Integration Technology Conference ESTC**
Rolf Aschenbrenner, General Chair of ESTC 2010, Klaus-Dieter Lang, Executive Chair of ESTC 2010
- 09:50 am** **KEYNOTE: Growing Importance of System Integration**
R. Ploss, Infineon Technologies AG
- 10:30 am** **KEYNOTE: Latest Panasonic Packaging Technology and Solutions**
Kiyoshi Arita, Panasonic Factory Solutions Co., Ltd.
- 11:10 am** **KEYNOTE: Packaging Trends in Mobile Electronics Towards Wafer Level Packaging**
Xavier Baraton, STMicroelectronics

■■■■■■■■■■ **Session: Modeling and Simulation (MS-1) – Power and RF**
Chair: Bernd Michel, Fraunhofer IZM, Fraunhofer ENAS, Germany, Co-Chair: J. Auersperg, AMIC GmbH, Germany

- 01:20 pm** **Accurate 3D Electromagnetic Simulation of RF System-in-Package**
N.-H. Huynh, K. Pressel, B. Roemer, Infineon Technologies AG, Neubiberg, Germany
- 01:45 pm** **Modular Modeling Approach to Consider RF and Thermal Behavior of Complex Systems Built up Using Interconnect Structures in 3D Integration**
S. Reitz, J. Stolle, R. Martin, A. Wilde, P. Schneider, Fraunhofer Institute for Integrated Circuits, Division Design Automation Dresden, Germany
- 02:10 pm** **Simulation of Power Delivery Networks with Joule Heating Effects for 3D Integration**
M. Swaminathan, J. Xie, Georgia Institute of Technology, Atlanta, USA
- 02:35 pm** **Thermal Test Vehicle for the Validation of Thermal Modelling of Hot Spot Dissipation in 3D Stacked ICs**
H. Oprins, V. Cherman, C. Torregiani, M. Stucchi, B. Vandeveld, IMEC, Leuven, Belgium

■■■■■■■■■■ **Session: Advanced Packaging (AP-1) – 3D Integration and RF-Packaging**
Chair: Klaus Pressel, Infineon Technologies AG, Germany; Co-Chair: Rajiv Dunne, TI, USA

- 01:20 pm** **3D IC Infrastructure Status and Issues**
J. Vardaman, TechSearch International, Inc., Austin, USA
- 01:45 pm** **Hermetic Wafer-Level Packaging Technology Development for RF MEMS Switch**
C. Ferrandon, CEA - MINATEC, Grenoble, France
- 02:10 pm** **Integration of a 3D Microwave Module**
X. Sun, P. Soussan, A. La Manna, B. Majeed, W. De Raedt, IMEC, Leuven, Belgium
- 02:35 pm** **TSV as an Alternative to Wire Bonding for a Wireless Industrial Product: Another Step towards 3D Integration**
G. Druais, E. Saugier, STMicroelectronics, Leuven, Belgium

■■■■■■■■■■ **Session: Applied Reliability (AR-1) – Solder Interconnect**
Chair: Kouchi Zhang, Philips, The Netherlands; Co-Chair: Y. F. Jin, Beijing University, China

- 01:20 pm** **Failure Mechanism of Solder Interconnections under Thermal Cycling Conditions**
T. Mattila, Aalto University, Espoo, Finland; M. Mueller, TU Dresden, Germany; M. Paulasto-Kröckel, Aalto, Finland; K.-J. Wolter, TU Dresden, Germany
- 01:45 pm** **Influence of Indium on Microstructure and Creep Properties of SnAg3.5InX (X=0,2,4,8) Solder Alloys**
J. C. Boareto, Universidade Federal de Santa Catarina, Florianópolis, Brazil; R. Metasch, Universität Dresden, Germany; M. Roellig, Fraunhofer IZfP, Dresden, Germany; P. A. Pereira Wendhausen, Universidade Federal de Santa Catarina, Florianópolis, Brazil; K.-J. Wolter, Universität Dresden, Germany
- 02:10 pm** **Solder Joint Reliability in Automotive Applications: Describing Understanding Damage Mechanisms through the Use of EBSD**
A. Steller, H. Baker INTEQ GmbH, Celle; U. Pape, Volkswagen AG, Wolfsburg; R. Dudek, Fraunhofer ENAS & IZM, Micro Materials Center Berlin/Chemnitz, Germany
- 02:35 pm** **Impact of Thermal Aging on the Thermal Fatigue Durability and Interfacial Intermetallic Compounds Thickness in Pb-free Solder Joints**
P. Chauhan, University of Maryland, College Park, USA; M. Mueller, TU Dresden, Germany; M. Osterman, M. Pecht, CALCE Electronic Products & Systems Center, College Park, USA

■■■■■■■■■■ **Session: Electrical Design & Modeling (ED-1)**
Chair: Günter Elst, Fraunhofer IIS, Germany; Co-Chair: Stephan Guttowski, Fraunhofer IZM, Germany

- 01:20 pm** **Current Density Simulations for Polymer Cored CSP Interconnects**
D. Whalley, Loughborough University / Conpart AS, UK; H. Kristiansen, Conpart AS, Skjetten, Norway
- 01:45 pm** **Passive Parametric Modeling of Interconnects and Packaging Components from Sampled Impedance, Admittance or Scattering Data**
P. Triverio, S. Grivet-Talocia, Politecnico di Torino, Italy; M. Nakhla, Carleton University, Ottawa, Canada
- 02:10 pm** **Crosstalk Analysis in High Density Connector Via Pin Fields for Digital Backplane Applications Using a 12-Port Vector Network Analyzer**
M. Kotzev, TU Hamburg-Harburg; R. Frech, H. Harrer, D. Kaller, A. Huber, T.-M. Winkel, IBM Deutschland Research & Development GmbH; H.-D. Brüns, C. Schuster, TU Hamburg-Harburg, Germany
- 02:35 pm** **Modeling and Analysis of Coplanar Bonding Wires for High-Speed Applications**
I. Ndip, C. Tschoban, S. Schmidt, M. Schneider-Ramelow, S. Guttowski, K.-D. Lang, H. Reichl, Fraunhofer IZM, Berlin, Germany

■■■■■■■■■■ **Session: Assembly and Manufacturing Technology (AM-1) – Assembly Technologies**
Chair: David Whalley, University of Loughborough, UK; Co-Chair: Gordon Elger, Phillips, Germany

- 01:20 pm** **Flip Chip Bonding with Elasticity Bonding System and Non Conductive Film Suitable for InterMetallic Compounds Formation;**
R. Kojima, T. Matsumura, T. Saito, T. Koyama, N. Umetsu, J. Nishimura, K. Furuta, Sony Chemical & Information Device Corp., Kanuma, Japan
- 01:45 pm** **Au-Sn Fluxless SLID Bonding: Effect of Bonding Temperature for Stability at High Temperature, above 400 °C**
K. E Aasmundtveit, T. Thuy Luu, H. Vu Nguyen, HVE Vestfold University College, Tonsberg; R. Johannessen, SINTEF ICT, Trondheim; N. Hoivik; K. Wang, HVE Vestfold University College, Tonsberg, Norway
- 02:10 pm** **Adapted Assembly Processes for Flip-Chip Technology with Solder Bumps of 50 µm or 40 µm Diameter**
R. Dohle, Micro Systems Engineering GmbH, Berg; F. Schübler, J. Franke, University of Erlangen-Nuremberg; T. Friedrich, J. Goßler, Micro Systems Engineering GmbH, Berg, Germany
- 02:35 pm** **Influence of the Processing Method on the Amount and Development of Voids in Miniaturized Interconnections**
D. Biljana, R. Labie, B. Verlinden, I. De Wolf, IMEC, Leuven, Belgium

Tuesday, September 14, 2010
04.00 pm – 05.40 pm

■■■■■■■■■■ Session: Modeling and Simulation (MS-2) – Reliability Applications I

Chair: Kikuo Kishimoto, Tokyo Institute of Technology, Japan; Co-Chair: Jürgen Keller, AMIC, Germany

- 04:00 pm** **Virtual Qualification - the Step into a New Period of Automotive Electronic Development**
A. Schiebl, D. Wolf, Continental Automotive GmbH
- 04:25 pm** **Rapid Virtual Testing of Structural Integrity in Microelectronic Assemblies**
Hossein Shirangi, C. Otto, A. Fischer, P. van Staa, Robert Bosch GmbH, Stuttgart; W. H. Müller, TU Berlin; B. Michel, Fraunhofer IZM- MMCB, Chemnitz, Germany
- 04:50 pm** **Adhesion of Moulding Compounds on Various Surfaces. A Study on Moisture Influence and Degradation after High Temperature Storage**
R. Pufall, M. Goroll, Infineon Technologies AG, Neubiberg; M. Bouazza, O. Wittler, B. Michel, Fraunhofer IZM Berlin, Germany
- 05:15 pm** **Highly Integrated Advanced Power Electronic Systems for Automotive Applications**
J.-P. Sommer, Fraunhofer ENAS, Chemnitz; T. Hofmann, Conti Temic microelectronic GmbH, Nuremberg; A. Neumann, Electronic AG, Schramberg; A. Podlasly, Fraunhofer IZM, Berlin; B. Michel, Fraunhofer IZM + ENAS, Germany

■■■■■■■■■■ Session: Advanced Packaging (AP-2) – Wafer Level

Chair: Jürgen Wolf, Fraunhofer IZM, Germany; Co-Chair: Jan Vardaman, TechSearch International, USA

- 04:00 pm** **Thin Wafer Processing and Chip Stacking for 3D Integration**
T. Matthias, B. Kim, M. Wimplinger, P. Lindner, EV Group, St. Florian am Inn, Austria
- 04:25 pm** **Eutectic Wafer Bonding for 3D Integration**
M. Baum, M. Wiemer, Fraunhofer ENAS, Chemnitz; A. Schneider, H. Rank, A. Trautmann, Robert Bosch GmbH, Gerlingen-Schillerhöhe; T. Gessner, Fraunhofer ENAS & Chemnitz University of Technology, Germany
- 04:50 pm** **Wafer-to-Wafer Hybrid Bonding Technology for 3D IC**
Cheng-Ta Ko, Zhi-Cheng Hsiao, Huan-Chun Fu, Kuan-Neng Chen, Wei-Chung Lo, Yu-Hua Chen, Industrial Technology Research Institute, Hsinchu, Taiwan
- 05:15 pm** **Technology Trends in the Manufacturing and Packaging of Wafer Level Cameras**
R. Zoberbier, SUSS MicroTec, Garching; A. Kraft, DELO Adhesives, Windach; R. Voelkel, D. Toennies, SUSS MicroTec, Garching, Germany

■■■■■■■■■■ Session: Applied Reliability (AR-2) – Solder Microstructures

Chair: Hans-Jürgen Albrecht, Siemens, Germany, Co-Chair: Matthias Hutter, Fraunhofer IZM, Germany

- 04:00 pm** **The Scaling Effect on Microstructure and Creep Properties of Sn-Based Solders**
S. Wiese, Fraunhofer CSP, Halle; M. Mueller, J. Panchenko, R. Metasch, K.-J. Wolter, TU Dresden; M. Roellig, Fraunhofer IzfP, Dresden, Germany
- 04:25 pm** **On the Role of Electromigration in Power Cycling Tests**
V. Vuorinen, J. Karppinen, T. Laurila, M. Paulasto-Kröckel, Aalto University, Espoo, Finland; A. Paul, Indian Institute of Science, Bangalore, India
- 04:50 pm** **Employing Solder Joints of Concave Shape for Monitoring Electromigration Independently of Material Interfaces**
J. Jaeschke, W. H. Müller, TU Berlin; N. Nissen, Fraunhofer IZM; H. Reichl, TU Berlin, Germany

■■■■■■■■■■ Session: Electrical Design & Modeling (ED-2) – 3D Related Modeling

Chair: Peter Schneider, Fraunhofer IIS, Germany, Co-Chair: Ivan Ndip, Fraunhofer IZM, Germany

- 04:00 pm** **Power Integrity Analysis by Using a Coupled Field-Circuit Method**
E. Li, Singapore A*STAR Institute of High Performance Computing, Fusionopolis, Singapore
- 04:25 pm** **TSV Modeling and Noise Coupling in 3D IC**
J. Kim, J. Cho, J. Kim, KAIST, Daejeon, South Korea
- 04:50 pm** **Electrical Evaluation of Wafer Level Fan Out (WLFO) Package Using Organic Substrate for Microwave Applications**
S.J. Lee, S.W. Kim, G.W. Kim, K.C. Bae, J.H. Yu, J.Y. Kim, H.Y. Yoo, C.H. Lee, Amkor Technology Korea, Seoul, South Korea

■■■■■■■■■■ Session: Assembly and Manufacturing Technology (AM-2) – Thin / Flexible System

Chair: Marc Desmulliez, Heriot Watt University, UK; Co-Chair: Christine Kallmayer, Fraunhofer IZM, Germany

- 04:00 pm** **Packaging Challenges Associated with Warpage of Ultra-Thin Chips**
Mahadi-UI Hassan, E. Angelopoulos, H. Rempp, S. Endler, J. Burghartz, Institute for Microelectronics Stuttgart (IMS CHIPS), Germany
- 04:25 pm** **Ultra-flexible and Ultra-Thin Embedded Medical Devices on Large Area Panels**
G. Kunkel, T. Debski, H. Burkard, J. Link, Hightec MC AG, Lenzburg, Switzerland; A. E. Petersen, Oticon A/S, Smorum, Denmark; W. Christiaens, J. Vanfleteren, IMEC, Gent, Belgium
- 04:50 pm** **Thin Die / Novel Process for Stack Die Packages and Yield Optimization**
T. Stoeckli, Kulicke & Soffa Industries Inc., Fort Washington, USA
- 05:15 pm** **Flexible Substrates and Stamped Circuit Board Technology**
M. Benedikt, Heraeus, Hanau, Germany

Wednesday, September 15, 2010
08.30 am – 10.10 am

■■■■■■■■■■ **Session: Modeling and Simulation (MS-3) – Reliability Testing and Simulation II**
Chair: Leo Ernst, Delft University of Technology, The Netherlands. Co-Chair: R. Dudek, Fraunhofer ENAS, Germany

- 08:30 am** **Modeling and Validation of Evaluation Method on IC Chip Pick-up Performance**
N. Saiki, K. Inaba, K. Kishimoto, Tokyo Institute of Technology; H. Senoo, K. Ebe, LINTEC Corporation, Tokyo, Japan
- 08:55 am** **Underfill and Mold Compound Influence on PoP Ageing Under High Current and High Temperature Stresses**
L. Meinshausen, K. Weide-Zaage, LfL Leibniz Universität Hannover, Germany; H. Fremont, Laboratoire IMS Université Bordeaux I, Talence, France
- 09:20 am** **Reliability Study of the Stud Bump Bonding Flip Chip Technology on Molded Interconnect Devices**
M. Dressler, Bosch, Waiblingen; B. Wunderle, TU Chemnitz; K. F. Becker, H. Reichl, Fraunhofer IZM, Berlin, Germany
- 09:45 am** **Interface Fracture Mechanics Evaluation by Correlation of Experiment and Simulation**
J. Keller, I. Maus, AMIC Angewandte Micro-Messtechnik GmbH, Berlin; B. Wunderle, B. Michel, Micro Material Center Berlin, Fraunhofer IZM, Germany

■■■■■■■■■■ **Session: Microsystem Packaging (MP-1) – Sensor Integration Issues**
Chair: Werner Wilke, VDI/VDE-IT, Germany; Co-Chair: Paradiso Coskina, VDI/VDE-IT, Germany

- 08:30 am** **In-situ Test Structures for Ultra Low Leak Detection**
S. Millar, M. Desmulliez, Heriot-Watt University, Edinburgh, UK; S. McCracken, MCS Ltd.
- 08:55 am** **Hermeticity of Eutectic Bond Layers for Sensor Packages on Wafer-Level**
A. Schneider, H. Rank, R. Müller-Fiedler, Robert Bosch GmbH, Gerlingen-Schillerhöhe; O. Wittler, Fraunhofer IZM, Berlin; H. Reichl, TU Berlin, Germany
- 09:20 am** **Fluxless Wafer Level Cu–Sn Bonding for Micro- and Nanosystems Packaging**
N. Hoiwik, K. Wang, K. Aasmundtveit, G. Salomonsen, HVE Vestfold University College, IMST - Faculty of Science and Engineering, Tonsberg; A. Lapadatu, G. Kittilsland, B. Stark, Sensoron ASA, Horten, Norway

■■■■■■■■■■ **Session: Applied Reliability (AR-3) – Material and Reliability**
Chair: Hélène Frémont, IXL Labs/CNRS, France; Co-Chair: Tadatomo Suga, Uni Tokyo, Japan

- 08:30 am** **Influence of Solder and Pad Coating Constitution on Fatigue of Lead-free Solder Joints under Combined Vibration and Temperature Cycling Loading**
P. Matkowski, J. Felba, Wrocław University of Technology, Faculty of Microsystem Electronics and Photonics, Wrocław, Poland
- 08:55 am** **Investigation of Adhesive Bonding on Base Metal in Electronic Packaging**
A. Paproth, TU Dresden IAVT; B. Adolphi, TU Dresden IHM; K.-J. Wolter, TU Dresden IAVT, Germany
- 09:20 am** **fibDAC Stress Relief – a Novel Stress Measurement Approach with High Spatial Resolution**
D. Vogel, I. Maus, B. Michel, Fraunhofer ENAS, Chemnitz, Germany
- 09:45 am** **New Test Bench to Test the Reliability of Electronics Boards**
K. Moreau, M. Grieu, C. Munier, EADS France IW, Suresnes, France

■■■■■■■■■■ **Session: New Materials and Processes (NM-1) – Die Attach**
Chair: Jan Felba, University of Wrocław, Poland; Co-Chair: Tanja Braun, Fraunhofer IZM, Germany

- 08:30 am** **Die-Attach for High-Temperature Applications Using Fineplacer-Pressure-Sintering (FPS)**
J. Kähler, A. Stranz, N. Heuck, G. Palm, A. Waag, E. Peiner, TU Braunschweig/Institute of Semiconductor Technology, Brunswick, Germany
- 08:55 am** **Investigations on Zn-Al-Ge Alloys as a High Temperature Die Attach Material**
A.S.M.A Haseeb, A. Haque, University of Malaya, Kuala Lumpur, Malaysia; W. Yunsung, ON Semiconductor, SCG Industries Malaysia Sdn Bhd, Seremban, W. Malaysia; M. i Hj. Hassan, University of Malaya, Kuala Lumpur, Malaysia
- 09:20 am** **New Silver Contact Pastes - From High Pressure Sintering to Low Pressure Sintering**
W. Schmitt, T. Krebs, WCH Heraeus GmbH, Hanau, Germany
- 09:45 am** **Thermal Conductivity in the Vertical Direction of Heat-Resistant Epoxy Based Conductive Adhesives with Multimodal Filler Size Distributions**
M. Inoue, Osaka University, Japan; J. Liu, Chalmers University of Technology, Göteborg, Sweden

■■■■■■■■■■ **Session: Assembly and Manufacturing Technology (AM-3) – RF-Packaging and Manufacturing Optimization**
Chair: Paul Svasta, Politehnica University of Bucharest, Romania; Co-Chair: Grace O'Malley, iNEMI, Ireland

- 08:30 am** **Investigation of RFID Tag Antennas Printed on Flexible Substrates Using Two Types of Conductive Pastes**
K. Janeczka, G. Koziol, T. Serzysko, Tele & Radio Research Institute, Warsaw, Poland
- 08:55 am** **Experimental Investigation of Open-Ended Microwave Oven Assisted Encapsulation Process for Quad Flat Packages**
S. Kumar Pavuluri, Heriot-Watt University, Edinburgh, UK; M. Ferenets, Eesti Innovatsiooni Instituut, Tallinn, Estonia; G. Goussetis, ECIT, Queen's University Belfast; M. Desmulliez, Heriot-Watt University, Edinburgh, UK; T. Tillford, University of Greenwich, UK; R. Adamietz, F. Eicher, Fraunhofer IPA, Stuttgart, Germany; C. Bailey, University of Greenwich, UK
- 09:20 am** **High Yield Thermode Bond Process Under Activated Atmosphere and Automatic Thermal Interface Measurement for High Power Optoelectronic Devices**
G. Elger, R. Lauterbach, R. Feder, K. Dankwart, Philips Technology GmbH, Global Technology Development Mechanization, Aachen; J. Matthyssen, Philips Technology GmbH, Global Technology Development Mechanization, Turnhout; C. Zilkens, Philips Technology GmbH, Global Technology Development Mechanization, Aachen, Germany
- 09:45 am** **Self-Assembly and Self-Interconnection of Thin RFID Devices on Plasma-Programmed Foil Substrates**
E. Yacoub-George, W. Hell, S. Scherbaum, C. Landesberger, K. Bock, Fraunhofer Research Institution for Modular Solid State Technologies, EMFT, Munich, Germany

Wednesday, September 15, 2010
11.00 am – 12.40 pm

■■■■■■■■■■ Session: Modeling and Simulation (MS-4) – Reliability Testing and Simulation I

Chair: Reinhard Pufall, Infineon Technologies AG, Germany; Co-Chair: Hossein Shirangi, Bosch, Germany

- 11:00 am** **Characterizing the Hardening Behavior of Copper and Gold Free Air Balls Using Micro Compression Test**
G. Lorenz, C. Dresbach, M. Petzold, Fraunhofer IWM, Halle, Germany
- 11:25 am** **A Microscope System for Characterization of Mechanical Properties of Small-Scaled Objects**
H. Tohmyoh, M. A. Salam Akanda, M. Saka, Tohoku University, Sendai, Japan
- 11:50 am** **Application of Multi-criteria Optimization Algorithms to Numerical Material Extraction of Thin Layers Through Nanoindentation Technique**
L. Dowhan, A. Wymysowski, Wroclaw University of Technology, Poland; P. Janus, M. Ekwirska, Institute of Electron Technology, Warsaw, Poland; Olaf Wittler, Fraunhofer IZM, Germany
- 12:15 pm** **Crack and Damage Evaluation in low-k BEoL Stacks under Assembly and CPI Aspects**
J. Auersperg, Fraunhofer ENAS and AMIC GmbH, Berlin; D. Vogel, Fraunhofer ENAS, Chemnitz and Fraunhofer IZM, Berlin; M. U. Lehr, M. Grillberger, Globalfoundries Dresden Module One LLC & Co. KG; B. Michel, Fraunhofer ENAS, Chemnitz and Fraunhofer IZM, Berlin, Germany

■■■■■■■■■■ Session: Microsystem Packaging (MP-2) – Microsystem Packaging

Chair: Markku Tilli, Okmetic, Finland; Co-Chair: Stéphane Renard, Tronics, France

- 11:00 am** **Future High Security ID-Documents Based on Innovative Micro System Technologies**
J. Kloeser, Bundesdruckerei GmbH, Berlin, Germany
- 11:25 am** **Biocompatibility Assessment of Advanced Wafer-level Based Chip Encapsulation**
M. Op de Beeck, E. Dy, R. Vos, A. La Manna, IMEC, Leuven, Belgium
- 11:50 am** **Influence of Accelerated Aging on the Acoustic Properties of a Ceramic Microsystem for Structural Health Monitoring**
S. Hildebrandt, B. Boehme, K.-J. Wolter, TU Dresden, IAVT, Germany
- 12:15 pm** **Polymer Bonding by Induction Heating for Microfluidic Applications**
C. Liu, B. J. Knauf, D. Patrick Webb, Paul P. Conway, Loughborough University, UK

■■■■■■■■■■ Session: Emerging Technologies (ET-1) – Wearables

Chair: Klaus-Jürgen Wolter, TU Dresden, Germany; Co-Chair: Changqing Liu, Loughborough University, UK

- 11:00 am** **Flipchip Bonding of Ultrahin Si Dies onto PEN/PET Substrates with Low Cost Circuitry**
J. van den Brand, R. Kusters, B. van Remoortere, A. Dietzel, Holst Centre / TNO, Eindhoven, The Netherlands
- 11:25 am** **Fundamental Analysis of Embroidered Interconnections for Electronics in Textiles**
T. Linz, S. Erik, H. Walter, Fraunhofer IZM, Berlin, Germany
- 11:50 am** **Stretchable Electronics Manufacturing and Application**
A. Ostmann, Fraunhofer IZM, Berlin; M. Seckel, T. Loehner, TU Berlin, Germany
- 12:15 pm** **Development of a Thin-Film Stretchable Electrical Interconnection Technology for Biocompatible Applications**
R. Verplancke, T. Sterken, F. Axisa, J. Vanfleteren, Ghent University - IMEC, Ghent, Belgium

■■■■■■■■■■ Session: New Materials and Processes (NM-2) – Material Analysis

Chair: Markus Detert, Otto-von-Guericke University Magdeburg, Germany; Co-Chair: Hans Walter, Fraunhofer IZM, Germany

- 11:00 am** **A Novel Approach for Reliability Assurance of Solder Pastes Against Dew Condensation**
J. Franke, C. Matzner, M. Rösch, Institute for Manufacturing Automation and Production Systems (FAPS), Erlangen, Germany
- 11:25 am** **Spherical Polymer Particles in Isotropic Conductive Adhesives - A Study on Rheology and Mechanical Aspects**
Hoang-Vu Nguyen, Vestfold University College, Borre, Norway; H. Kristiansen, Conpart AS, Skjetten, Norway; J. Gakkestad, Norwegian Defence Research Establishment, Kjeller, Norway; R. Johannessen, SINTEF ICT, Oslo, Norway; N. Hoivik, K. Aasmundtveit, Vestfold University College, Borre, Norway
- 11:50 am** **Water Diffusion in Micro- and Nano-particle Filled Encapsulants**
T. Braun, J. Bauer, Fraunhofer IZM, Berlin; L. Georgi, TU Berlin; K.-F. Becker, M. Koch, V. Bader, R. Aschenbrenner, Fraunhofer IZM, Berlin; H. Reichl, TU Berlin, Germany
- 12:15 pm** **Properties of High-k Materials Embedded in Low Temperature Cofired Ceramics**
H. Bartsch, J. Müller, R. Grieseler, TU Ilmenau; S. Barth, B. Pawlowski, IKTS Hermsdorf, Germany

■■■■■■■■■■ Session: Assembly and Manufacturing Technology (AM-4) – Wire Bonding

Chair: Bernd Appelt, ASE, USA; Co-Chair: Stefan Schmitz, Fraunhofer IZM, Germany

- 11:00 am** **Aluminium Wedge-Wedge Wire Bonding on Thermoplastic Substrates Made by LPKF-LDS® Technology**
P. Buckmüller, HSG-IMAT, Stuttgart, Germany
- 11:25 am** **Fine Pitch Copper Wire Bonding Introduction to High Volume Production**
B. Appelt, A. Tseng, ASE (U.S.) Inc., Gulf breeze, USA; Y.-S. Lai, ASE Kaohsiung, Taiwan
- 11:50 am** **Enabling High Volume Copper Wire Bonding With Enhancements to Process and Equipment Capability**
B. Chylak, J. Foley, H. Clauberg, Kulicke & Soffa Industries, Fort Washington, USA
- 12:15 pm** **Elastic Properties of Bonding Wires**
C. Dresbach, M. Mittag, P. Matthias, Fraunhofer IWM, Halle, Germany

Wednesday, September 15, 2010
02.00 pm – 03.40 pm

IMAPS Europe's Global Business Council

Chair: Roland Müller-Fiedler, Bosch, Germany; Co-Chair: Zsolt Illyefalvi-Vitez, University of Budapest, Hungary

02:00 pm Needs for Micro-Electronics in Active Implantable Cardiac Devices

Alain Ripart PhD FHRS, Senior Vice President, Chief Scientific Officer, Sorin CRM

02:25 pm The Interconnect Foundry Concept in Modern Medical Electronics

Michael A. Fink, CEO, DYCONEX AG

02:50 pm Managing Reliability Expectations & Warranty Costs in Medical Electronics

Cheryl Tulkoff, Senior Member of the Technical Staff at DfR Solutions

03:15 pm High Reliable Silicon Capacitors for Medical Applications

Catherine Bunel, R&D Director, IPDiA

Session: Modeling and Simulation (MS-5) – Reliability Applications II

Chair: Rainer Dudek, Fraunhofer ENAS, Germany; Co-Chair: Lukasz Dowhan, Wroclaw University of Technology, Poland

02:00 pm Mechanical Issues Induced by Electrical Wafer Sort: Correlations from Actual Tests, Nanoindentation and 3D Dynamic Modeling

R. Roucou, V. Fiori, F. Cacho, STMicroelectronics; Karim Inal, Xavier Boddaert, Ecole Nationale Supérieure des Mines de Saint Etienne, France

02:25 pm Device Simulation for Evaluating Effects of Mechanical Stress on Semiconductor Devices: Impact of Stress-induced Variation of Electron Effective Mass

M. Koganemaru, Fukuoka Industrial Technology Center, Kitakyushu; K. Yoshida, T. Ikeda, N. Miyazaki, Kyoto University; Hajime Tomokage, Fukuoka University, Japan

02:50 pm Fracture Analysis of Interface Delamination in Metal-Insulator-Metal Capacitor Device

M.-C. Hsieh, Industrial Technology Research Institute, Hsinchu; T.-L. Kuo, C. Hwu, National Cheng Kung University, Taiwan

03:15 pm Multi-Physics Modelling for Packaging of Liquid Crystal Displays in Harsh Environments

C. Bailey, L. Hua, Y. Chunyan, L. Yek, University of Greenwich, UK

Session: Microsystem Packaging (MP-3) – Processes

Chair: Roland Müller-Fiedler, Bosch, Germany; Co-Chair: Zsolt Illyefalvi-Vitez, University of Budapest, Hungary

02:00 pm 3D Welding of Ultrathin Pt Wires by Joule Heating

S. Fukui, H. Tohmyoh, M. Saka, Department of Nanomechanics, Tohoku University, Sendai, Japan

02:25 pm Aerosol Printed High Definition Co-Fired Metallization Lines for LTCC-Packages

U. Partsch, S. Mosch, M. Ihle, Fraunhofer IKTS, Dresden, Germany

02:50 pm Low cost Thin Film Packaging for MEMS Overmolded

J.-L. Pornin, C. Gillot, C. Billard, E. Lagoutte, M. Pellat, G. Parat, N. Sillon, CEA-LETI-MINATEC, Grenoble, France

03:15 pm Characterization of Surface Profile for Surface Activated Bonding by Using Power Spectral Density Function

K. Tsukamoto, T. Suga, The University of Tokyo, Japan

Session: Emerging Technologies (ET-2) – Detector / PV

Chair: Toni Mattila, TU Helsinki, Finland; Co-Chair: Ricky Lee, Hong Kong University of Science and Technology, China

02:00 pm Micro Electrode Array for Electrical Recording of Membrane Ionic Currents

A. Aryasomayajula, J. Derix, S. Perike, G. Gerlach, R. Funk, TU Dresden, Germany

02:25 pm X-Ray Resistant Packaging for X-Ray Line Detectors

M. Oppermann, T. Lohse, R. Metasch, T. Zerna, K.-J. Wolter, TU Dresden / Electronics Packaging Lab., Dresden, Germany

02:50 pm Packaging Technologies for Photovoltaic Modules – Technological Challenges and Mechanical Integrity

S. Wiese, Fraunhofer CSP, Halle; N. Betzl, D. Wald, Solarwatt, Dresden; F. Kraemer, R. Meier, Fraunhofer CSP, Halle, Germany

03:15 pm Development of Charged Particle Detectors by Integrating Gas Amplification Stage and CMOS ASIC on Wafer Level

J. Kaminski, Universität Bonn; T. Baumgartner, Fraunhofer IZM, Berlin; K. Desch, Universität Bonn; O. Ehrmann, T. Fritzsche, Fraunhofer IZM, Berlin; T. Krautscheid, Universität Bonn; S. Mayer, M. Töpfer, Fraunhofer IZM, Berlin, Germany

Session: New Materials and Processes (NM-3) – Material Deposition

Chair: James E. Morris, Portland State University, USA; Co-Chair: Karl-Friedrich Becker, Fraunhofer IZM, Germany

02:00 pm Characterisation of Silver Particles Used for the Low Temperature Joining Technology

C. Früh, M. Günther, M. Rittner, Robert Bosch GmbH, Schwieberdingen; M. Nowottnick, Universität Rostock, Germany

02:25 pm Aerosol Deposition of Catalytic Ink to Fabricate Fine Pitch Metallizations for Moulded Interconnect Devices (MIDs)

A. Brose, T. Leneke, S. Hirsch, B. Schmidt, Otto-von-Guericke-University Magdeburg, Germany

02:50 pm Rapid Prototyping of Electronic Modules Combining Aerosol Printing and Ink Jet Printing

H. A. Gieser, H. Wolf, D. Bonfert, H. Hengelmann, Fraunhofer EMFT, München, V. Zöllmer, Ch. Werner, Fraunhofer IFAM, Bremen; G. Domann, J. Bahr, Fraunhofer ISC, Würzburg; B. Curran, I. Ndip, K. Bock, Fraunhofer IZM, Berlin, Germany

03:15 pm Influence of Nano Silver Filler Content on Properties of Ink-Jet Printed Structures for Microelectronics

T. Falat, J. Felba, Wroclaw University of Technology, Poland; A. Moscicki, A. Smolarek, Amepox Microelectronics, Lodz, Poland; K. Bock, D. Bonfert, Fraunhofer EMFT, München, Germany

Session: Assembly and Manufacturing Technology (AM-5) – Substrates

Chair: Jörg Franke, Friedrich-Alexander-University Erlangen-Nürnberg, Germany;

Co-Chair: Andreas Ostmann, Fraunhofer IZM, Germany

02:00 pm Frames, Cavities & Channels – Advanced Mechanical Structures in PCBs

C. Lehnberger, Andus Electronic GmbH, Berlin, Germany

02:25 pm Novel Hermetic and Low Cost Glass-Capping Technology for Wafer-Level-Packaging of Optical Devices

U. Hansen, S. Maus, J. Leib, MSG Lithoglas AG; M. Toepper, Fraunhofer IZM, Berlin, Germany

02:50 pm The Benefits of Pure Palladium with ENEP and ENEPIG Surface Finishes

M. Özkök, Atotech Deutschland GmbH, Berlin, Germany

03:15 pm MEMS Tightly Sealed with SCHOTT HermeS substrates

G. Todt, SCHOTT Electronic Packaging, Landshut, Germany

Wednesday, September 15, 2010
04.30 pm – 06.10 pm

■■■■■■■■■■ Session: Modeling and Simulation (MS-6) – Thermal Management

Chair: Chris Bailey, University of Greenwich, UK; Co-Chair: Ralf Schacht, FH Lausitz, Germany

- 04:30 pm** **MDS Investigation on the Heat Transfer Properties of CNT Micro-Channel Cooler**
Y. Zhang, S. Wang, J.-Y. Fan, Shanghai University, China; Johan Liu, Chalmers University of Technology, Göteborg, Sweden
- 04:55 pm** **On Model Fitting Methods for Analysis of Polymer Cure Kinetics in Microelectronics Assembly Applications**
J. E. Morris, Portland State University, Portland, USA; T. Tilford, University of Greenwich, London, UK; M. Ferenets, Eesti Innovatsiooni Instituut, Tallinn, Estonia; P. R. Rajaguru, University of Greenwich, London, UK; S. Pavuluri, M. P. Y. Desmulliez, Heriot-Watt University, Edinburgh, UK; C. Bailey, University of Greenwich, London, UK
- 05:20 pm** **Simulation of Electro-Thermal Interaction**
A. Wilde, R. Jancke, A. Wilde, R. Martin, S. Reitz, P. Schneider, Fraunhofer IIS/EAS, Dresden, Germany

■■■■■■■■■■ Session: Advanced Packaging (AP-3) – 2nd Level Interconnect

Chair: Eric Beyne, IMEC, Belgium; Co-Chair: Michel Garnier, STMicroelectronics, France

- 04:30 pm** **3D Substrate Innovation for Complex High Pin Count Flip-Chip Applications**
V. Solberg, V. Oganessian, Tessera/STC-Madison, San Jose, USA
- 04:55 pm** **Reliability Improvements for Large Scale Wafer Level Packaging**
J. Hunt, ASE (US) Inc, Tempe, USA; D. Huang, J. Chiu, MaggieMC Liu, J. Lin, JW Lo, C. Chen, G. Kao, ASE Group
- 05:20 pm** **Reliability Testing of Cu-Sn Intermetallic Micro-Bump Interconnections for 3D-Device Stacking**
R. Labie, P. Limaye, IMEC, Leuven, Belgium; K. Wook Lee, AMKOR Korea; CJ Berry, AMKOR US; E. Beyne, I. De Wolf, IMEC, Leuven, Belgium
- 05:45 pm** **Process Integration of Fine Pitch Micro-Bumping and Cu Redistribution Wiring for Power Efficient SiP**
H. Ezawa, T. Migita, S. Yamashita, Y. Koshio, M. Fukuda, Toshiba Corporation Semiconductor Company, Yokohama; T. Togasaki, Toshiba Corporation; M. Miyita, K. Nagamine, T. Iijima, Toshiba Corporation Semiconductor Company, Yokohama, Japan

■■■■■■■■■■ Session: Applied Reliability (AR-4) – Experiment and Testing

Chair: W. J. Sander Gielen, TNO, The Netherlands; Co-Chair: Dietmar Vogel, Fraunhofer ENAS, Germany

- 04:30 pm** **Development of a Mechanical Stress-Analysing-Tool to Characterize Packaging Processes**
S. Höll, S. Majcherek, S. Hirsch, B. Schmidt, Otto-von-Guericke University Magdeburg, Germany
- 04:55 pm** **Localization and Analysis of Subsurface Defects at Flip-Chip- and Fully Packaged Multi-Chip-Devices**
C. Schmidt, C. Große, F. Altmann, Fraunhofer IWM, Halle, Germany
- 05:20 pm** **Experimental Damage Analysis and Numerical Reliability Modeling of Lead-Free Ball-Grid-Array Second Level Interconnects**
D. Pustan, J. Wilde, Z. Wenxin, University of Freiburg - IMTEK, Freiburg, Germany
- 05:45 pm** **Effect Mechanism of Moisture Diffusion on LED Reliability**
X. Luo, B. Wu, L. Sheng, Huazhong University of Science and Technology, Wuhan, China

■■■■■■■■■■ Session: New Materials and Processes (NM-4) – Soldering Processes

Chair: Mervi Paulasto, Helsinki University of Technology, Finland; Co-Chair: Hermann Oppermann, Fraunhofer IZM, Germany

- 04:30 pm** **Newly Developed Low Cost, Reliable Wafer Level Hermetic Sealing Using Cu/Sn System**
Yu D.Q., Institute of Microelectronics, CAS, P. R. China; Thew M. L., Institute of Microelectronics, A*STAR, Singapore
- 04:55 am** **Nanoscaled Solder for Low-Temperature Assembling Processes**
A. Novikov, M. Nowottnick, University of Rostock, Institute of Electronic Appliances and Circuits, Germany
- 05:20 am** **Electrolytic Solder Deposit for Next Generation Flip Chip Solder Bumping**
B. Roelfs, S. Kenny, Atotech Deutschland GmbH, Germany

■■■■■■■■■■ Session: Assembly and Manufacturing Technology (AM-6) – Inspection and Test

Chair: Erik Jung, Fraunhofer IZM, Germany; Co-Chair: Jürgen Leib, MSG Lithoglas, Germany

- 04:30 pm** **Ceramic Injection Molded Clevis Sensor for Online Substance Concentration Measurement**
M. Hartmann, S. Doerner, S. Hirsch, Otto-von-Guericke University of Magdeburg, Germany
- 04:55 pm** **Inspection of Through Silicon Vias (TSV) in IC Packages by Computed Tomography**
H. Roth, Z. He, T. Mayer, GE Sensing & Inspection Technologies GmbH, Germany
- 05:20 pm** **Changes of the Coplanarity of SMT-Components during Soldering and their Measurement**
H. Wohlrabe, TU Dresden ZµP; K.-J. Wolter, TU Dresden IAVT, Germany
- 05:45 pm** **Report on iNEMI Boundary Scan Adoption Project Results and Future Plans**
G. O'Malley, H. Fu, iNEMI, Ireland; P. B. Geiger, Dell Inc.; S. Butkovich, Cisco Systems Inc.

Thursday, September 16, 2010
08.30 am – 10.10 am

■■■■■■■■■■ Session: New Materials and Processes (NM-5) – Nanomaterials

Chair: Johan Liu, Chalmers University Gothenborg, Sweden, Co-Chair: Michael Töpfer, Fraunhofer IZM, Germany

- 08:30 am** **Polymeric Nanocomposites for Advanced Electronic and Photonic Packaging Applications**
C. P. Wong, R. Zhang, Y. Liu, J. Moon, O. Hildreth, J. Agar, Georgia Institute of Technology, Atlanta, USA
- 08:55 am** **Nanoporous Interconnects**
H. Oppermann, L. Dietrich, M. Klein, Fraunhofer IZM, Berlin, Germany
- 09:20 am** **Interpenetrating Phase Polymer-Metal Composite for Thermal Interface Material Applications**
B. Carlberg, J. Liu, Chalmers University of Technology, Göteborg, Sweden & Shanghai University, Mechatronical Engineering and Automation Building, Shanghai, China
- 09:45 am** **Surface Activated Bonding between Au substrate and Vertically Aligned Multiwalled Carbon Nanotubes**
M. Fujino, T. Suga, The University of Tokyo; I. Soga, D. Kondo, Y. Ishizuki, T. Iwai, M. Masataka, Fujitsu Laboratory / Fujitsu Ltd., Japan

■■■■■■■■■■ Session: Advanced Packaging (AP-4) – Technologies

Chair: Thomas Zerna, TU Dresden, Germany; Co-Chair: Bradford Factor, ASE

- 08:30 am** **Stacked Anodized Metal Substrate for High Thermal Dissipation Performance**
C.H. Lim, Y.K. Lee, K.H. Seo, J.W. Kim, S.M. Choi, Samsung Electro-Mechanics, Suwon, South Korea
- 08:55 am** **Wire-Bonding on Inkjet-Printed Silver Pads Reinforced by Electroless Plating for Chip on Flexible Board Packages**
R. Cauchois, Gemalto / Ecole Nationale Supérieure des Mines de St-Etienne; M. Saadaoui, J. Legeleux, Ecole Nationale Supérieure des Mines de St-Etienne; T. Malia, B. Dubois-Bonvalot, Gemalto; K. Inal, Ecole Nationale Supérieure des Mines de St-Etienne; J.-C. Fidalgo, Gemalto, France
- 09:20 am** **Low Profile CSP (LP-CSP) Technology for Ultra-Thin IC Packaging Applications**
U. Sharma, ON Semiconductor
- 09:45 am** **Module Miniaturization by Ultra Thin Package Stacking**
T. Loeher, D. Schütze, TU Berlin, Deutschland; W. Christiaens, K. Dhaenens, Swarnakamal Priyabadini, IMEC Ghent, Belgium; A. Ostmann, Fraunhofer IZM, Berlin, Germany; J. Vanfleteren, IMEC Ghent, Belgium

■■■■■■■■■■ Session: Applied Reliability (AR-5) – Moisture / Microstructure

Chair: Bernhard Wunderle, Fraunhofer ENAS, Germany; Co-Chair: Detlef Bonfert, Fraunhofer EMFT, Germany

- 08:30 am** **EBSD Microstructure Investigations of Electronic Materials down to the Nanoscale**
M. Krause, B. März, C. Dresbach, M. Petzold, Fraunhofer IWMH, Halle; T. Oppert, PacTech GmbH, Nauen, Germany
- 08:55 am** **Understanding Die Attach Materials Performance in Electronic Packages under Harsh Environments**
M. Sousa, University of Oxford; S. Riches, GE Aviation-Newmarket, Suffolk; C. Johnston, P. S. Grant, University of Oxford, UK
- 09:20 am** **A Novel Vapor Pressure Transfusion Model for the Popcorning Analysis of Quad Flat No-lead (QFN) Packages**
M. Zhang, S.-W. R. Lee, The Hong Kong University of Science and Technology, Kowloon, Hong Kong
- 09:45 am** **Experimental Methods for Analysis of Humidity Sensitive Material Properties of Microelectronic Relevant Polymers**
H. Walter, MMCB at Fraunhofer IZM, Berlin; H. Shirangi, Bosch MAHLE Turbo Systems, Stuttgart; B. Wunderle, Technical University of Chemnitz; E. Dermitzaki, MMCB at Fraunhofer IZM, Berlin; B. Michel, MMC at Fraunhofer ENAS, Chemnitz, Germany

■■■■■■■■■■ Session: Optoelectronics (OE-1) – Lighting and Laser

Chair: Harri Kopola, VTT, Finland; Co-Chair: Ulrich Fischer-Hirchert, University of Applied Science Wernigerode, Germany

- 08:30 am** **Microbench for Optical Pulse Picking from 4 GHz Pulse Trains by Mode Locking of DBR Lasers**
A. Klehr, A. Liero, T. Hoffmann, J. Schulz, S. Schwertfeger, H. Wenzel, G. Erbert, W. Heinrich, G. Tränkle, Ferdinand-Braun-Institut, Berlin, Germany
- 08:55 am** **Integrated LED modules**
M. de Samber, E. van Grunsven, E. Eggink, Philips Applied Technologies, Eindhoven, Netherlands; W. Peels, Philips Lighting LightLabs
- 09:20 am** **Injection Moulded Lens Array for High Power LED Modules**
E. Juntunen, A. Keränen, VTT Technical Research Centre of Finland, Oulu; M. Paakkinen, V. Vuorinen, E. Tetri, L. Halonen, Aalto University School of Science and Technology, Espoo; Veli Heikkinen, VTT Technical Research Centre of Finland, Finland
- 09:45 am** **Integration of a Multifunctional and Multiwavelength Optical Sensor for Automotive Applications Using Surface Mountable Planar Optical Interconnects**
A. Klein, G. Jordan, S. Marx, H. Schröder, H. Oppermann, Fraunhofer IZM, Berlin, Germany; D. Capello, N. Pallaro, Fiat Research Center CRF

■■■■■■■■■■ Session: Power Electronics (PE-1) – Thermal Issues

Chair: Martin Schneider-Ramelow, Fraunhofer IZM, Germany; Co-Chair: Frank Osterwald, Danfoss Silicon Power GmbH

- 08:30 am** **Thermal Optimisation of GaN Flip Chip Power Transistors**
R. Zhytnytska, O. Hilt, V. Sidorov, J. Würfl, G. Tränkle, Ferdinand-Braun-Institut Leibniz-Institut für Höchstfrequenztechnik, Berlin, Germany
- 08:55 am** **Thermal and Mechanical Design Optimization of a Pressure-Mounted Base-Plate-less High Temperature Power Module**
N. Matthey, R. Skuriat, J. Li, P. Agyakwa, C. M. Johnson, University of Nottingham, UK
- 09:20 am** **Thermal Modeling for Advanced High Power Packaging Development and Online Performance Monitoring**
C. Yuan, TNO IenT; J. Salta, P. Dirks, NXP Semiconductors, Eindhoven; W. van Driel, Technology University of Delft, The Netherlands
- 09:45 am** **Power Cycling Tests at High Temperatures with IGBT Power Modules for Hybrid Electrical Vehicle Applications**
A. Hensler, J. Lutz, Chemnitz University of Technology; M. Thoben, J. Zachariae, Infineon Technologies AG, Warstein, Germany

Thursday, September 16, 2010
11.00 am – 12.40 pm

■■■■■■■■■■ Session: New Materials and Processes (NM-6) – Materials Characterization

Chair: Paul Conway, Loughborough University, UK, Co-Chair: Jürgen Auersperg, AMIC GmbH, Germany

- 11:00 am** **Thermomechanical Analysis of Electrically Conductive Adhesives**
P. Mach, D. Bu_ek, CTU Prague, Faculty of Electrical Engineering, Prague, Czech Republic
- 11:25 am** **Use of Non-Etching Adhesion Promoters in Advanced PCB Applications**
R. Massey, A. Zee, Atotech GmbH, Berlin, Germany
- 11:50 am** **Anodic Bonding at Low Voltage using Microstructured Borosilicate Glass Thin-Films**
J. Leib, U. Hansen, S. Maus, MSG Lithoglas AG, Berlin; H. Feindt, TU Hamburg-Harburg; M. Toepper, Fraunhofer IZM, Berlin, Germany

■■■■■■■■■■ Session: Advanced Packaging (AP-5) – Embedding

Chair: Gilles Poupon, Leti, France; Co-Chair: Coen Tak, NXP, The Netherlands

- 11:00 am** **System Integration with eWLB**
T. Meyer, G. Ofner, B. Römer, Infineon Technologies AG, Regensburg, Germany
- 11:25 am** **Fan-Out Wafer-Level Packaging with Highly Flexible Design Capability**
Y. Kurita, T. Kimura, K. Shibuya, H. Kobayashi, F. Kawashiro, N. Motohashi, M. Kawano, NEC Electronics Corporation, Sagami-hara, Japan
- 11:50 am** **A Novel Approach to Embed off-Chip RF Passives Based on Thin Film Technology**
L. Wang, W. Christiaens, J. Vanfleteren, Ghent University, Centre for Microsystems Technology, Ghent, Belgium
- 12:15 pm** **Implementation of Chip Embedding Processes for the Creation of Miniaturized System-in-Packages**
L. Boettcher, Fraunhofer IZM, Berlin; D. Manassis, TU Berlin; A. Ostmann, Fraunhofer IZM, Berlin;
S. Karaszkiwicz, TU Berlin, Germany

■■■■■■■■■■ Session: Applied Reliability (AR-6) – Stress and Strain

Chair: André Rouzaud, Leti, France; Co-Chair: Matthias Petzold, Fraunhofer IWM, Germany

- 11:00 am** **Formation of Mechanical Strains in the Component Board of a High-end Handheld Product during Shock Impact**
J. Karppinen, J. Pakarinen, J. Li, T. Mattila, M. Paulasto-Kröckel, Aalto University, Espoo, Finland
- 11:25 am** **Electrical Stress on Film Resistive Structures on Flexible Substrates**
D. Bonfert, G. Klink, H. Gieser, K. Bock, Fraunhofer EMFT, München, Germany; P. Svasta, Ciprian Ionescu, University Politehnica, Bucharest, Romania
- 11:50 am** **Advanced Assessment of Thermal Stress Related Failure Modes Occurring During the Assembly of High Pin Count BGAs on PCBs**
M. Hertl, D. Weidmann, Insidix, Seyssins, France
- 12:15 pm** **Investigation into the Impact of Component Floor Plan Layout on the Overall Reliability of Electronics Systems in Harsh Environments**
D. Braden, Delphi Electronics Group, Liverpool; D. Harvey, G.-M. Zhang, R. Yang, Liverpool John Moores University; J. Duralek, Delphi Electronics & Safety, Liverpool, UK

■■■■■■■■■■ Session: Optoelectronics (OE-2) – Data Transmission and Display

Chair: Giovanni del Rosso, Cogo Optronics, Germany; Co-Chair: Xiaobing Luo, Wuhan National Lab for Optoelectronics, China

- 11:00 am** **Active Optical Flex Module for Ultra-Short Distance Data Applications**
M. Immonen, Meadville Group, Salo, Finland; J. Wu, P. Cheng, Y.H. Luo, Shanghai Meadville Science and Technology, China; H. He, W. Huang, J.X. Xu, Shanghai Meadville Electronics Co., Ltd., China; Tarja Rapala-Virtanen, Guangzhou Meadville Electronics Co. Ltd., China
- 11:25 am** **New Method for Head-up Display Realization by Mean of Chip On Board and Aerosol Jet Process**
S. Padovani, S. Sinesi, S. Priante, M. Antonipieri, A. Del Negro, Centro Ricerche Plast-optica S.p.A., Amaro, Italy; V. Zoellmer, M. Maiwald, Fraunhofer IFAM, Bremen, Germany; M. Hedges, Neotech Services MTP, Nuremberg, Germany
- 11:50 am** **Microelectronic-like Packaging for Silicon Photonics: a 10 Gbps Multi-Chip-Module, Optical Receiver Based on Ge-on-Si Photodiode**
S. Bernabé, C. Kopp, J.-M. Fedeli, L. Lombard, CEA- LETI-MINATEC, Grenoble, France
- 12:15 pm** **A Small Form-Factor and Low-Cost Opto-Electronic Package for Short-Reach 40 Gbit/sec Serial Speed Optical Data Links**
J.-R. Kropp, J. A. Lott, N. N. Ledentsov, VI-Systems GmbH Berlin; P. Otruba, EZconn Europe GmbH Berlin; K. Drögemüller, ix-cad GmbH, Eichenau; G. Fiol, D. Birnberg, TU Berlin; I. Ndip, R. Erxleben, Fraunhofer IZM, Berlin, Germany

■■■■■■■■■■ Session: Power Electronics (PE-2) – Materials

Chair: Thomas Harder, ECPE, Germany; Co-Chair: Markus Thoben, Infineon Technologies AG, Germany

- 11:00 am** **Ceramic Substrates with Aluminium Metallisation for Power Application**
H. Knoll, W. Weidenauer, P. Ingram, IXYS Semiconductor GmbH, Lampertheim; S. Bennemann, M. Petzold, Fraunhofer IWM, Halle, Germany
- 11:25 am** **Transfer Layer Technology for the Packaging of High Power Modules**
M. Balucani, P. Nenzi, R. Crescenzi, University of Rome, Italy; L. Dolgyi, A. Klyshko, V. Bondarenko, Belarussian State University of Informatics and Radioelectronics, Minsk, Belarus
- 11:50 am** **Impact of Printed Circuit Board Technology on Thermal Performance of High-Power LED Assembly – Experimental Results**
J. Nicolics, Vienna University of Technology, Vienna, Austria; G. Langer, F. Lutschounig, AT&S, Austria Technologie und Systemtechnik AG Klagenfurt Leiterplatten GmbH, Klagenfurt, Germany; K.-J. Lang, R. Huber, OSRAM Opto Semiconductors GmbH, Regensburg, Germany
- 12:15 pm** **Integrated Magnetics on Silicon for Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC)**
C. Ó Mathúna, N. Ning Wang, Tyndall National Institute, Cork, Ireland

Thursday, September 16, 2010
01.40 pm – 02.30 pm

- 01.40 pm **Keynote: Micro-Technologies for New Neural Interfaces: Current Status and Future Prospects**
Eduardo Fernández, University Miguel Hernandez, Spain
- 02.20 pm **Presentation of ESTC 2010 Best Paper Presentation Award and ESTC 2010 Best Poster Award**
- 02.30 pm **Closing Ceremony**

Tuesday, September 14, 2010
03.00 pm – 04.00 pm

Poster Session 1

Label-free Chemical/Biochemical Sensing Device Based on an Integrated Microfluidic Channel within a Waveguide Resonator

E. McKeever, S. Pavuluri, R. Lopez-Villarroya, D. Kavanagh, M. Desmulliez, Heriot Watt University, Edinburgh, UK

Surface Modification and Wettability of Silicone Polydimethylsiloxane Films

K-Y Wang, G-M Ouyang, X-Y Chen, Institute for Microsystem, Vestfold University College, Borre, Norway

Board Level Reliability with Strain-Controllable Dynamic Bending Method for Green IC Packaging Validation

L. Jeffrey, ChangBing, Yu Chi-Ko, Chang Graver, Shao Tina, IST-Integrated Service Technology Inc. Hsinchu, Taiwan

New Facts from Lead-free Solders Reliability Investigation

I. Szendiuch, J. Jankovsky, M. Bursik, Brno University of Technology, Brno, Czech Republic

FPGA-Board and Active Optical Cable Design for Optical Multi-Gigabit Communication

F. Merchán, K.-H. Brenner, ziti Universität Heidelberg; P. Gregorius, S.-H. Voß, Fraunhofer-Institut für Nachrichtentechnik, Heinrich-Hertz-Institut, Berlin, Germany

Fabrication and Test of Arrays of Langasite Microbalances

E. Ansorge, A. Brose, B. Schmidt, University Magdeburg; J. Sauerwald, H. Fritze, TU Clausthal, Germany

Testing and Simulation of Wire Bonding Attach for Higher Current Density

M. Bursik, E. Hejatkova, J. Jankovsky, M. Novotny, I. Szendiuch, Brno University of Technology, Brno, Czech Republic

Thermodynamic Sensors – New Opportunities for Measuring and Control in Industrial Applications

M. Reznicek, I. Szendiuch, Brno University of Technology; Z. Reznicek, HIT Ltd., Brno, Czech Republic

Organic humidity sensors - Improvement of climatic resistance

J. Reboun, A. Hamacek, T. Dzugan, M. Kroupa, University of West Bohemia, Pilsen, Czech Republic

Controlling the Signal Integrity Through the Geometry of the Microstrip on the Digital PCBs

M. Zolog, D. Pitica, Technical University of Cluj-Napoca, Romania

Assembly Requirements for Multi-Channel Coupling Micro-Optics in Board-Level Optical Interconnects

K. Nieweglowski, R. Rieske, K.-J. Wolter, TU Dresden, Electronics Packaging Laboratory, Germany

Modeling and Design of Packing Power Delivery System with Embedded Discrete Capacitor

H.-H. Cheng, C.-W. Kuo, National Sun Yat-Sen University, Kaohsiung, Taiwan; P.-C. Pan, C.-Y. Huang, C.-C. Wang, C.-T. Chiu, Advanced Semiconductor Engineering

Properties and Growth of Intermetallics Formed During Thermal Aging of Cu-Al Ball Bonds

M. Kouters, F. Gubbels, TNO Science & Industry, Eindhoven, The Netherlands

Numerical Analysis of Microwave-Assisted Quad-Flat Package Encapsulation Processes

T. Tilford, University of Greenwich, UK; M. Ferenets, Eesti Innovatsiooni Instituut, Tallinn, Estonia; R. Adamietz, Fraunhofer IPA, Stuttgart, Germany; S. Pavuluri, Heriot-Watt University, Edinburgh, UK; J. E. Morris, Portland State University, USA; M. P. Y. Desmulliez, Heriot-Watt University, Edinburgh, UK; C. Bailey, University of Greenwich, UK

On the Integration of Microwave Curing Systems into Microelectronics Assembly Processes

R. Adamietz, G. Müller, N. Othman, F. Eicher, Fraunhofer IPA, Stuttgart, Germany; T. Tilford, University of Greenwich, UK; M. Ferenets, Eesti Innovatsiooni Instituut, Tallinn, Estonia; S. Pavuluri, M. P. Y. Desmulliez, Heriot-Watt University, Edinburgh, UK; C. Bailey, University of Greenwich, UK

Silver Nanocluster Formation Using Ultra-violet Radiation for Direct Metal Patterning on Polyimide

D. E. Watson, J. Hoyd-Gigg Ng, M. Desmulliez, MISEC, Heriot Watt University, Edinburgh, UK

Simulation and Parameter Optimization of Power DMOS Trench Field Effect Transistors

V. Baranov, Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus; A. Belous, M. Krechko, I. Roubtsevich, V. Siakerski, A. Tourtsevich, Integral Corporation, Naperville, USA

The Connecting of Electronic Modules Using SMD Components' Package

J. Sandera, O. Svecova, Brno University of Technology, Department of Microelectronics, Brno, Czech Republic

Electrical characterization of PEDOT: PSS

S. Pretl, M. Kroupa, A. Hamacek, T. Dzugan, J. Reboun, J. Cengery, The University of West Bohemia, Pilsen, Czech Republic

Novel Event Detector and Data Acquisition System for Accelerated Reliability Tests of Interconnections

P. Matkowski, K. Urbanski, Wroclaw University of Technology, Wroclaw, Poland; J. Felba, M. Pecht, M. Osterman, CALCE, University of Maryland, College Park, USA; R. Zawierta, Wroclaw University of Technology, Wroclaw, Poland

Wednesday, September 15, 2010
10.10 am – 11.00 am

Poster Session 2

Modeling of Ultrasonic Microwelding System by Finite Element Method

V. Lanin, I. Petuchov, D. Buchalko, Belarus State University of Informatics and Radioelectronics, Minsk, Belarus

Epoxy Resin Curing Process Evaluation based on Signal Frequency Analysis from Interdigital Structure Sensor

T. Blecha, J. Pihera, University of West Bohemia, Pilsen, Czech Republic

Determination of Maximum Strength and Optimization of LED Chip Structure

S.-Y. Yang, T.-L. Chou, C.-F. Huang, K.-N. Chiang, National Tsing Hua University, Hsinchu, Taiwan

Growth Behaviour of Gold-aluminum Intermetallic Phases (IMP) in Temperature Aged Ball Bonds Observed by Electron Backscatter Diffraction

B. März, S. Scheibe, A. Graff, M. Petzold, Fraunhofer IWM, Halle, Germany

Head on Pillow Defects in BGAs Solder Joints

A. Arazna, G. Koziol, W. Steplewski, K. Lipiec, Tele & Radio Research Institute, Warsaw, Poland

Influence of Metallographic Preparation on EBSD Characterization of Cu Wire Bonds

T. Zerna, A. Tkachenko, M. Müller, K.-J. Wolter, TU Dresden, Germany

Microstructure and Mechanical Properties of Laser Ablation Cleaned NiP-Platings for Aluminum Wire Bonding

S. Benemann, C. Dresbach, G. Lorenz, L. Berthold, M. Petzold, Fraunhofer IWM, Halle, Germany

Design and Implementation of an Integrated RF System-in-Package for Healthcare Applications

F. Wagner, N. Abo Elneel, D. Schroeder, W. Krautschneider, Hamburg University of Technology, Germany

A Series of New SAC Solder Paste of Better Performance with the Nanosilver Powder and Nanocarbon Tubes Additives

M. Jakubowska, W. Niedzwiedz, Warsaw University of Technology; K. Bukat, M. Koscielski, J. Sitek, Tele Radio Institute, Warsaw; A. Mlozniak, Institute of Electronic Materials Technology, Warsaw, Poland

Injection Moulded Key Components for Integrated WDM POF Communication Systems

U.H.P. Fischer, M. Haupt, Harz University of Applied Sciences, Wernigerode, Germany

Local Stress Measurement Methods for Packaging Purposes– A Comparison

A. Gollhardt, D. Vogel, B. Michel, Fraunhofer ENAS, Chemnitz, Germany

Fine Pitch Cu/Sn Solid State Diffusion Bonding for Making High Yield Bump Interconnections and its Application in 3D Integration

W. Zhang, P. Limaye, Y. Civalie, R. Labie, P. Soussan, IMEC, Leuven, Belgium

A New Type of Cone-shaped High Gain Circularly Polarized Antenna for PCB Integration

C.-C. Liu, ITRI, Hsinchu, Taiwan

Characterization Methods for Determination of Temperature Depended Electrical, Thermal, Mechanical and Fatigue Properties of SnAg3,5 Solder

M. Roellig, Fraunhofer Institut for Non-Destructive Testing; R. Metasch, K. Meier, Electronics Packagaing Laboratory; F. Alt, Fraunhofer Institut for Non-Destructive Testing, Dresden, Germany

Inertial Bridge with on Board Digital Signal Processing

P. Mugur Svasta, I.-A. Hapenciuc, CETTI, Bucharest, Romania

Project VISA PCB Based Fully Integrated Power Electronic Systems for Automotive Electronics

T. Hofmann, Continental AG, Nuremberg, Germany

Through Silicon Via Polymer Filling for 3D-WLP Applications

M. Bouchoucha, STMicroelectronics; P. Chausse, CEA-LETI; L.-L. Chapelon, STMicroelectronics; St. Moreau, N. Sillon, CEA-LETI, Grenoble, France

Reliability of Solder Joints Assessed by Acoustic Imaging During Accelerated Thermal Cycling

R. S. H. Yang, D. M. Harvey, Z. Guang-Ming, Liverpool John Moores University; D.R. Braden, Delphi Electronics Group, Liverpool, UK

Reliability Evaluation of Silver InkJet Printed Traces

R. Bonadiman, Nokia Institute; M. Salazar, University of the State of Amazonas, Manaus, Brazil

Impacts of Uniaxial Mechanical Stress on High Frequency Performance of MOSFETs

Y.-G. Han, Fukuoka Science & Technology Foundation; M. Koganemaru, Fukuoka Industrial Technology Center; W. Choi, H. Tomokage, Fukuoka University, Japan

Backlight Illumination Structure Based on Inorganic LED Devices and Laminated Multilayer Polymer Substrate

K. Keränen, M. Heikkinen, J. Rekilä, A. Sunnari, M. Hiltunen, K. Rönkä, VTT Printed Functional Solutions, Oulu, Finland

Root Cause Analysis Support for Quality Improvement in the High Value Added Printed Circuit Assembly (PCA) Manufacturing

L. A. Huertas-Quintero, P. P. Conway, D. M. Segura-Velandia, A. A. West, Loughborough University, UK

Aurispo - A Highly Integrated Platform for 24/7 Monitoring of Vital Data

E. Jung, Fraunhofer IZM, Berlin, Germany

Influences of Soldering Processes on Piezoelectric Properties

S. Bramlage, S. Walter, K.-J. Wolter, Electronics Packaging Laboratory, TU Dresden, Germany

Wednesday, September 15, 2010
03.40 pm – 04.10 pm

Poster Session 3

Thermal Signal Behaviour for Air Flow Measurement as Fundamentals to Time-of-Flight

O. Ecin, E. Engelen, B. Strathen, R. Viga, Universität Duisburg-Essen; B. Hosticka, Fraunhofer Institut IMS, Duisburg; A. Grabmaier, Universität Duisburg-Essen, Germany

Boundary Condition Independent Multiple Cooling Surfaces Transient Compact Thermal Model

T. Azoui, P. Tounsi, J.-M. Dorkel, LAAS-CNRS, Toulouse, France

Progress Towards the Development of Novel Fabrication and Assembly Methods for the Next Generation of Ultrasonic Transducers

J. Hoyd-Gigg Ng, D. Flynn, Y. Lacrotte, M. Desmulliez, Heriot-Watt University, Edinburgh; R. Ssekitoleko, C. Démoré, S. Cochran, University of Dundee, UK

DoE Simulations with the MicroDAC-Stress-Chip for Material and Package Investigations

F. Schindler-Saefkow, Fraunhofer ENAS, Chemnitz; B. Wunderle, Technische Universität Chemnitz; B. Michel, Fraunhofer ENAS, Chemnitz, Germany

Ribbon Bonding in Power Modules

C. Luechinger, Kulicke & Soffa, Fort Washington, USA

RFID System for the Identification of Biological Samples

K. Hichri, H. Zimmermann, F. Ihmig, Fraunhofer IBMT, Sulzbach/Saar, Germany

Investigation of Misalignment in Microwave Multilayer Filters

W. Ali, H. Bunyan, College of Technological Studies, Hawalli, Kuwait

The Impact of Carbon Nanotubes Diameter on their Thermal Conductivity – Non-equilibrium Molecular Dynamics Approach

B. Platek, T. Falat, J. Felba, Wroclaw University of Technology, Poland

New Packaging Concept for Ultra High Precision 3D Tactile Probes for CMM Applications

S. Bueteifisch, Physikalisch Technische Bundesanstalt, Braunschweig, Germany; F. Solzbacher, University of Utah, Salt Lake City, USA; H. Danzebring, U. Brand, L. Koenders, Physikalisch Technische Bundesanstalt, Braunschweig, Germany

Reliability Improvement of a Powder Blasting Process for Micro-Machining Applications

Y. Lacrotte, Heriot-Watt University, Edinburgh, UK

Effects of Failure Criteria on the Constant Humidity Test Results

K. Kokko, L. Frisk, Tampere University of Technology, Tampere, Finland

Passive Assembly of Parallel Optical Interfaces onto Electro-Optical Printed Circuit Board

R. Pitwon, Xyratex Technology Ltd., Havant, UK

Improvement in Joint Reliability of SiC Power Devices at above 300°C by Modifying the DBC Substrate

F. Lang, H. Ohashi, H. Yamaguchi, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan

Electron Transport in Ta Nanolayers: Application to Tantalum Capacitors

M. Kopecký, M. Chvátal, V. Sedláková, Brno University of Technology, Czech Republic

Optimization of Lead-Free Wave Soldering Process Using Taguchi Orthogonal Arrays

P. Mach, S. Barto, CTU Prague, Faculty of Electrical Engineering, Czech Republic

Intermodulation Distortion as Indicator for Flip Chip Solder Joint Degradation

M. Krüger, TU Berlin; N. Nissen, Fraunhofer IZM, Berlin; H. Reichl, TU Berlin, Germany

Vapor-Assisted Low Temperature Bonding Method for Cu and SiO₂

A. Shigetou, National Institute for Materials Science, Ibaraki; T. Suga, The University of Tokyo, Japan

Introduction of Nanosized Al₂O₃ in Sn-Ag_{3.5} solders by Mechanical Alloying

J. C. Boareto, G. Rodrigues, M. Mastropieto, P. A. Pereira Wendhausen, Universidade Federal de Santa Catarina, Florianópolis, Brazil; K.-J. Wolter, Universität Dresden, Germany

A Detailed Investigation of the Failure Formation of Copper Trace Cracks During Drop Tests

F. Kraemer, Fraunhofer CSP, Halle; S. Rzepka, Fraunhofer ENAS, Chemnitz; S. Wiese, Fraunhofer CSP, Halle; W. Faust, Fraunhofer ENAS, Chemnitz; J. Lienig, TU Dresden, Germany

Freeform Lens for White LEDs with High Angular Color Uniformity

K. Wang, D. Wu, F. Chen, Z. Liu, X. Luo, S. Liu, Huazhong University of Science & Technology, Wuhan, China

RF – MEMS Devices First Order Packaging

W. Tschann, Reinhardt Microtech AG; P. Heeb, Interstate University of Applied Sciences of Technology Buchs; O. Bosholm, Reinhardt Microtech AG

Development of Sensor Nodes Employing LTCC- based Capacitive Pressure Sensors

C. Marghescu, C. Ionescu, C. Tamas, P. Svasta, UPB-CETTI, Bucharest, Romania

Investigation of Nano-Patterned PZT Thin Films by Piezoresponse Force Microscopy

M. Waegner, M. Hoffmann, A. Haußmann, G. Suchaneck, G. Gerlach, L. M. Eng, TU Dresden, Germany

Contactless Material Deposition by Jetting for Heterogeneous System Integration

K.-F. Becker, A. Kurz, H. Reichl, TU Berlin; M. Koch, J. Bauer, T. Braun, Fraunhofer IZM, Berlin, Germany

Thursday, September 16, 2010
10.10 am – 11.00 am

Poster Session 4

Fineline Structuring on LTCC-Substrates for HF-Components

D. Stöpel, S. Humbla, M. Mach, TU-Ilmenau, Germany

An Effect of Ageing Processes on Electroluminescent Parameters of Thick-Film Lighting Structures

M.I Ciez, Institute of Electron Technology, Warsaw; Z. Porada, Technical University Krakow, Poland

Board Design Optimization for Fine Pitch BGA Components

A. Géczy, Z. Illyefalvi-Vitéz, Budapest University of Technology and Economics, Hungary

Influence of Processing Conditions on Characteristics of LTCC Materials

K. Makarovic, Jozef Stefan Institute; A. Meden, Faculty of Chemistry and Chemical Technology; M. Hrovat, Jozef Stefan Institute; D. Belavic, HIPOT-RR d.o.o.; J. Holc, M. Kosec, Jozef Stefan Institute, Ljubljana, Slovenia

An IC Centric Biocompatible Chip Encapsulation Flow

M. Op de Beeck, A. La Manna, T. Buisson, E. Dy, P. Soussan, C. Van Hoof, IMEC, Leuven, Belgium

Analyses of Thermo Mechanically Related Failures of Raction IGBT Power Modules at Short Circuit Switching

B. Nagl, J. Nicolics, Vienna University of Technology, Austria

Analysis of Vapor Phase Soldering in Comparison with Conventional Soldering Technologies

Z. Illyefalvi-Vitéz, R. Bátorfi, P. Szoke, A. Géczy, M. Ruzinko, Budapest University of Technology and Economics, Hungary

Liquid Crystal Polymer as a Substrate Material for Flip Chip ACA Interconnections

L. Frisk, A. Parviainen, K. Kokko, Tampere University of Technology, Finland

A Brief Review of 2D and 3D Numerical Methods for Determination of Strain Energy Release Rate by Commercial FE Codes

M. Hossein Shirangi, Robert Bosch GmbH, Stuttgart; L. Fard-Samiei, TU Berlin; Metin Koyuncu, Robert Bosch GmbH, Stuttgart, Germany

The Polyboard Tool Kit – A Novel Hybrid Optical Board Technology to Build Small-sized Optical Components with Complex Functionality

M. Vitt, A. Thiel, FOC fibre optical components GmbH, Germany

A Simulation-Based Design Method to Transfer Surface Mount RF System to Flip-Chip Die Implementation

L.Zheng, A. Mathewson, B. O Flynn, M. Hayes, C. O Mathuna, Tyndall National Institute, Cork, Ireland

Reliability of Al and Au Wire Bonds to SiC Diodes Working Under Thermal Stress

R. Kisiel, Warsaw University of Technology, Poland

Low Temperature Hybrid Bonding Using Self-Alignment

J.H. Lee, T.H. Ha, C.W. Lee, C.D. Yoo, KAIST; J.Y. Song, Korea Institute of Machinery and Materials, Daejeon, South Korea

Investigation of Wettability and Interface Reactions of Sn-Pb, Sn-Ag-Pb and Sn-Ag-Cu Solders for Solar Cell Interconnections

S. Schindler, S. Wiese, Fraunhofer CSP, Halle, Germany

Rate Dependent Mechanical Behaviour of SAC Solder in Fast Tensile Experiments

K. Meier, TU Dresden, Germany

PCB Tracks Thermal Simulation, Analysis and Comparison to IPC-2152 for Electric Current Carrying Capacity

R. A. Bunea, P. Svasta, C. Ionescu, I. Plotog, University Politehnica of Bucharest, Pitesti, Romania

Required Cleanliness for Isotropically Electrically Conductive Adhesive Bonding of SMD Devices onto FR4 Circuit Boards and Inline-Capable Analysis of these Contamination Levels Prior to Adhesive Bonding

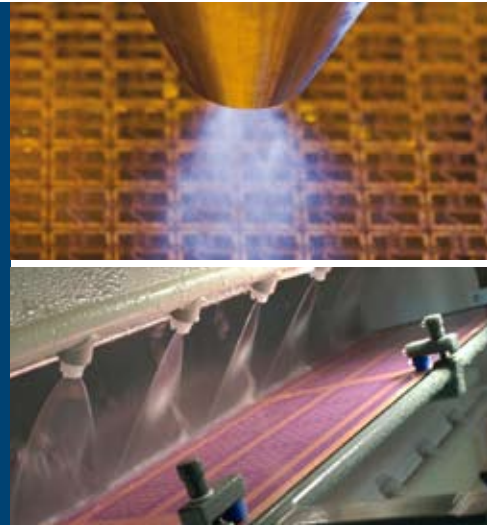
T. Gesang, S. Markus, Fraunhofer IFAM, Bremen; J. Haberland, Fraunhofer IZM, Berlin, Germany

The Development and Commercialization of a Unique Substrate Technology for the Radio Frequency (RF) Wireless and Cellular Module Market

D. Jandzinski, D. Leahy, J. Orłowski, M. Haji-Rahim, RFMD, Greensboro, USA

Thermo Mechanical Behaviour of Dies in Multi Material Stacks

M. Hintz, CiS Forschungsinstitut für Mikrosensorik und Photovoltaik, Erfurt; R. Dudek, Fraunhofer ENAS, Chemnitz; I. Koch, TU Ilmenau; F. Schindler-Saefkow, Fraunhofer ENAS, Chemnitz; A. Steinke, CiS Forschungsinstitut für Mikrosensorik und Photovoltaik, Erfurt, Germany



Top: Spray coating for thin film processes
Bottom: Substrate manufacturing line at Fraunhofer IZM

Technical Tour of Fraunhofer IZM Laboratories

Friday, September 17, 9:00 am - 01:00 pm, Fraunhofer IZM

Cost: EUR 45,- (includes lunch buffet)

To sign up, please send an email to [estc2010\(at\)mcc-pr.de](mailto:estc2010(at)mcc-pr.de).

On Friday, September 17, Fraunhofer IZM opens its doors for participants of ESTC 2010! Join us to see the state-of-the-art cleanroom, the recently established substrate manufacturing line and the laboratory for the integration of electronics into textiles!

Clean room and wafer level packaging line

Together with the Research Center for Microperipheral Technologies at Berlin's Technical University Fraunhofer IZM boasts a 800 m² clean room (classes 10 to 1000), with equipment for 4", 6" and 8" wafers, prototyping equipment for some applications is also available on 300 mm.

The focus is on thin-film deposition (sputter and evaporation), photolithography, galvanic bumping, circuit tracks and through-via filling (Cu, Ni, Au, AuSn, SnAg, PbSn), wet-chemical processes (etching, cleaning), wafer bonding (support wafer, thin-wafer handling) and silicon plasma etching (through vias, cavities).

Substrate manufacturing line

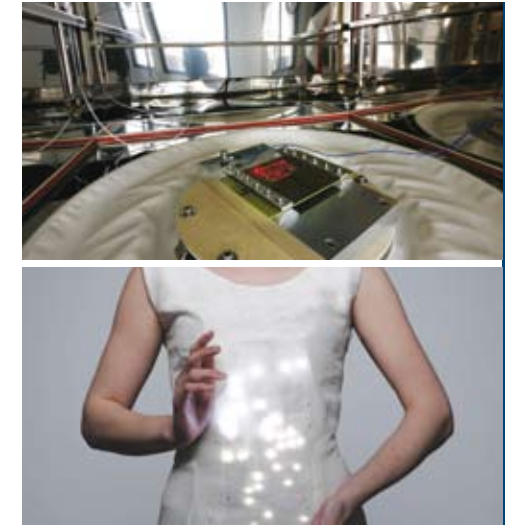
Fraunhofer IZM has recently designed and installed a new prototyping and process line for substrate manufacturing. Using the new equipment, substrates with a maximum size of 610 mm x 456 mm can be continuously processed. The process line features high-precision component placement, vacuum lamination press for multilayer fabrication and component embedding, UV laser drilling and structuring, mechanical drilling and milling, photolithographic patterning using laser direct imaging and dry-film photo resist, horizontal spray development of ultra-fine line structures, horizontal spray etching and photo-resist stripping, and automatic and manually operated galvanic equipment. As the equipment forms a continuous processing line the technology can be easily transferred to conventional industrial manufacturing environments. Moreover, it is also flexible enough to be adapted and varied for the development of new technologies.

Electronics Condition Monitoring Laboratory (ECM)

ECM specializes in function tests on electronic systems under environmental stress beyond purely thermomechanical strain. Combined testing processes are employed, such as vibration combined with humidity and/or temperature. The component's condition is determined precisely during testing using degradation-dependant parameters and by recording the stresses. The resulting data are compared with failure models and used for the design and testing of monitoring structures and to assemble condition indicators.

Textile Lab

In 2009 a new lab was launched at Fraunhofer IZM to concentrate the competencies and equipment for integrating electronics into textiles. Besides the many tools for assembly, reliability and analysis, additional equipment for textile processes and textile reliability tests has been installed. This includes a professional embroidery machine, a thermopress, a crimping machine, a washing machine for standardized testing and a tensile tester. The projects currently under development include applications for automotive interior, medical science, fashion design and logistics.



Top: Test stand for combined loading, including temperature (cycling), moisture and vibration
Bottom: Pneuma dress – The wearer's breathing pattern gives the lighting impulse for the electronics integrated into the dress

General Information

Conference Registration

The conference registration fee includes admission to all conference sessions, the poster sessions and the exhibition. The conference package includes an electronic copy of the proceedings, a list of registered conference participants and authors, lunch and refreshments during breaks. Regular participants (including speakers, poster presenters and session chairs, steering committee members and IEEE/IMAPS members) have free admission to the evening events. For students and accompanying persons extra tickets can be purchased for these events.

Conference Fees

	early bird (till June 30)	regular fee (from July 1)
Regular	595 EUR	720 EUR
Speaker	490 EUR	
IEEE, IMAPS Member	490 EUR	630 EUR
Session Chairs, Steering Comm.	490 EUR	
Students (limited number)	310 EUR	390 EUR
Events (students, spouses)		
Welcome Reception "Berliner Abend"	40 EUR	50 EUR
Gala Dinner "Meilenwerk"	85 EUR	100 EUR

Tutorials

Tutorial, full-day	425 EUR
Tutorial, half-day	295 EUR
Workshop, full-day	425 EUR

Payment and Cancellation

Payment should be marked "ESTC 2010" and must contain the name of the registrant. The registration fee may be credited towards the Fraunhofer IZM account no later than September 6, 2010. All transfer charges must be covered by the participant's bank.

Cancellation received in writing before August 16 will be subject to an administration charge of 60 EUR. No refund will be issued after August 15.

Conference Venue: Maritim proArte Hotel

The ESTC 2010 will be held at the Maritim proArte Hotel in Berlin. The Hotel is situated in Friedrichstraße, near the historic centre, not far from the Brandenburg Gate, the boulevard "Unter den Linden", and the Museum Island. You can easily get everywhere with the excellent public transport, or explore the "genuine" Berlin on foot, with its traditional pubs, fashionable restaurants and cultural highlights.

Rooms at preferential rates have been reserved for participants of the conference up to June 30th. September is a very busy time in Berlin, so reservations are highly recommended. Please use the ordering form on our website or mention the keyword "ESTC 2010" when making your reservation over the phone.

Maritim proArte Hotel Berlin
Friedrichstrasse 151, 10117 Berlin, Germany
Phone: + 49 (0) 30 2033-5
Fax: + 49 (0) 30 2033-4090
Reservation: + 49 (0) 30 2033-4410
E-Mail: info.bpa@maritim.de

Contact Information During the Conference

Phone: +49 30 2033-4301
Fax: +49 30 2033-4302

Conference Language and Proceedings

The official language of all presentations is English. The conference package will be handed out at the registration desk upon check-in.

ESTC 2010 Exhibition Services

Make the most of the ESTC 2010 Conference by presenting your technological products and services to decision-makers from research and industry at the concurrent exhibition! Located directly in front of the conference area, the exhibition is like the market place of a village - the center of communication. With a conference schedule designed to give visitors ample time to visit the stands, all break time catering and the poster exhibition will take place in this area. On more than 750 m2 exhibition area companies and research institutions will present new products and services.

Exhibition Stand Rental

There is a very limited number of stands still available. The offer includes: energy supply (220V), inscription of company's name (top) and company's logo (sideways), one table or counter, and two chairs.

Charges:

6 m² booth incl. conference admission for 1 person: 2,800,- € plus VAT

9 m² booth incl. conference admission for 1 person: 4,100,- € plus VAT

Exhibitors at ESTC 2010

- Bundesministerium für Bildung und Forschung, Germany
- centrotherm thermal solutions GmbH + Co. KG, Germany
- cyberTECHNOLOGIES GmbH, Germany
- Dage Deutschland GmbH
- Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration IZM, Germany
- Institut für Mikro- und Sensorsysteme (IMOS), Otto-von-Guericke-Universität Magdeburg, Germany
- KME Germany AG & Co. KG, Germany
- MicroContact AG, Switzerland
- Micro Systems Engineering GmbH, Germany
- Pac Tech Packaging Technologies GmbH, Germany
- Panasonic Industrial Europe GmbH, Germany
- PROTAVIC INTERNATIONAL, France
- SET - Smart Equipment Technology, France
- Sony Chemicals, Germany
- Süss MicroTech, Germany
- Tamarack Scientific Co., Inc., USA
- Tech Search International, USA
- WISTA Management GmbH
- XYZTEC bv, The Netherlands
- Yole Développement, France

Berlin... Germany's capital

When on November 9, 1989 the Berlin Wall came down and the Brandenburg Gate opened, a new chapter in the history of Berlin began. Parliament and Government moved to the German capital, embassies, media, companies, artists, lobby-organisations followed. The new Berlin can be seen at Potsdamer Platz, where a totally new quarter was built. The Reichstag was restored and received the famous "dome" designed by Sir Norman Foster. There are new buildings for the political institutions, new embassies and a new "Bundeskanzleramt", presently home to chancellor Angela Merkel. The new main train station in the Tiergarten district has added a new architectural highlight to the city skyline. The town is still full of construction sites.

Multicultural City

3.4 million people live in Berlin. Berlin is well known for its multitude of cultures, religions and life styles. People from more than 150 nations live here, among them the largest Turkish community outside Turkey, to which the Kreuzberg district owes its nickname "Little Istanbul". Each year in spring people from many nations show their traditions singing and dancing at the "Carnival of Cultures", which attracts more than half a million people. A walk through the 12 districts gives the best impression of this multicultural city.

Cultural hotspot

Opera or avant-garde performance, antique sculpture or surrealist painting, tradition or innovation - Berlin caters to all tastes. You have the choice between three Opera Houses. From the Staatsoper Unter den Linden it is a short walk to Museum Island (World Culture Heritage of UNESCO) where the Old Museum with Nefertiti, and the treasures of the Old National Gallery can be seen. The Jewish Museum in Kreuzberg gives an excellent impression of more than 2000 years of Jewish life. In the districts Mitte, Prenzlauer Berg, Friedrichshain and Kreuzberg the young, innovative scene can be found: galleries, fashion designers, musicians. These districts are also excellent places to go out at night - they offer a large variety of clubs, bars, restaurants. There is no closing time.

City of science

Four universities with more than 140,000 students are situated in Berlin. Besides the universities there are many other research institutes from the realms of applied and basic research, for example belonging to the Fraunhofer-Gesellschaft and the Max-Planck-Gesellschaft, as well as and two technology parks.

... and a great place for the ESTC 2010

The Maritim pro Arte Hotel is situated in Friedrichstraße, near the historic centre, not far from the Brandenburg Gate, the boulevard "Unter den Linden", and the Museum Island. You can easily get everywhere with the excellent public transport.

Contact

Conference Chair

Rolf Aschenbrenner
Phone: +49 30 46403-164
Fax: +49 30 46403-161
rolf.aschenbrenner@izm.fraunhofer.de

Organizing Team ESTC 2010

Fraunhofer IZM

Stefan Ast
Phone: +49 30 46403-130
Fax: +49 30 46403-131
estc2010@izm.fraunhofer.de

Ursula Mischke
Phone: +49 30 46403-160
Fax: +49 30 46403-161
estc2010@izm.fraunhofer.de

Conference Secretariat ESTC 2010 MCC Agentur für Kommunikation

Martina Creutzfeldt
Phone: +49 30 61.28.86.11
Fax: +49 30 61.28.86.88
email: estc2010@mcc-pr.de



Sponsored by



Berlin Adlershof

Heraeus



BOSCH

Panasonic
ideas for life



Organized by



