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Packaging Trends in Mobile Electronics – Towards Wafer Level Packaging

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Mobile electronics growth has recently been supported by the integration of more features for higher end devices. Smart phones are indeed growing at much faster pace than the overall mobile phone market. Requirements towards packaging are therefore asking breakthrough innovation to allow best package integration at optimized cost.

Wafer Level Packaging solutions (fan-in WLP and embedded wafer level packaging) are gaining growing interest as packaging technologies with many advantages in comparison to standard Ball Grid Array Packages, in particular with miniaturization of dice. Fan-in WLB is widely used for smaller packages because of its good electrical and thermal performance, highest package interconnect density and integration possibilities at lowest packaging cost. Fan-out embedded wafer level packaging is based on a reconstituted wafer which is built prior to the thin-film technology, adding space around the dice to increase the possible number of interconnects on the package. This Reconstituted Wafer is afterwards processed by applying dielectric, redistribution, passivation and solder balls in a modified thin-film and backend technology

Fan-out embedded wafer level packaging technology (eWLB) offers flexibility for more I/Os, multi-chips, and system integration. There are some restrictions in possible applications for Fan-In WLPs since global chip trends tend toward smaller chip areas with an increasing number of interconnects. The shrinkage of the pitches and pads at the chip to package interface is happening much faster than the shrinkage at the package to board interface. This interconnection gap requires fan-out packaging, where the package size is larger than the chip size in order to provide a sufficient area to accommodate the 2nd level interconnects. eWLB (embedded Wafer Level BGA) is a type of fan-out WLP that has the potential to realize any number of interconnects with standard pitches at any shrink stage of the wafer node technology.

Furthermore, 3D eWLB technology enables 3D IC and 3D SiP packaging with vertical interconnection. 3D eWLB can be implemented with through via on mold compound applications as well as discrete component embedding.

Recent progresses in 3D eWLB packaging and integration will be addressed in this paper as well as vision and future technology requirements in 3D packaging. The advantage of 3D eWLB technology and applications of 3D packaging will be presented with several examples. Some discussion around 3D eWLB fabrication process flow, assembly and packaging challenges, and performance characteristics will be also discussed.